

8-Bit CMOS *FlexROM*[™] Microcontrollers

Devices included in this data sheet:

- PIC16FR62A
- PIC16FR63
- PIC16FR64A
- PIC16FR65
- PIC16FR65A

PIC16FR6X Microcontroller Core Features:

- · High performance RISC CPU
- · Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC 20 MHz clock input DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- · Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- · Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS *FlexROM* technology

- Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- Commercial and Industrial Temperature Range
- Low-power consumption:
- < 2 mA @ 5V, 4 MHz
- 15 µA typical @ 3V, 32 kHz
- < 1 µA typical standby current</p>

PIC16FR6X Peripheral Features:

- · Timer0: 8-bit timer/counter with prescaler
- Timer1: 16-bit timer/counter with prescaler. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with period register, prescaler and postscaler
- Capture/Compare/PWM module(s)
- Capture is 16-bit, max resolution 12.5 ns, compare is 16-bit, max resolution 200 ns, max. PWM resolution is 10-bit.
- Synchronous Serial Port (SSP) with SPI and I²C[™]
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls
- Brown-out dectection circuitry for Brown-out Reset (BOR)

PIC16FR6X Features	62A	63	64A	65	65A
Program Memory (FlexROM)	2K	4K	2K	4K	4K
Data Memory (Bytes)	128	192	128	192	192
I/O Pins	22	22	33	33	33
Parallel Slave Port			Yes	Yes	Yes
Capture/Compare/PWM Module	1	2	1	2	2
Timer Modules	3	3	3	3	3
Serial Communication	SPI/I ² C	SPI/I ² C, USART	SPI/I ² C	SPI/I ² C, USART	SPI/I ² C, USART
Brown-out Reset	Yes	Yes	Yes	—	Yes
Interrupt Sources	7	10	8	11	11
Sink/Source Current (mA)	25/25	25/25	25/25	25/25	25/25

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1.0 GENERAL DESCRIPTION

The PIC16FR6X is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16FR6X microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16FR6X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16FR62A** devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus.

The **PIC16FR63** devices have 192 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/ Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also know as a Serial Communications Interface or SCI.

The **PIC16FR64A** devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/ Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16FR65** and **PIC16FR65A** devices have 192 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/ counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided. The PIC16FR6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and reset(s).

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lockup.

The PIC16FR6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The *FlexROM* technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16FR6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Code written for PIC16C5X can be easily ported to PIC16FR6X family of devices.

1.2 Development Support

The PIC16FR6X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer, and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16FR6X FAMILY OF DEVICES

				Clock		Memory		Peripl	Peripherals			Features
				(ATH)	- 1				()		\land	
				Jour Metto	. N			NO H	VA.			
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			o Tour	alon whe		1	e e	No.	40	1.		1000
			A no	, to		Yor Var			07.	42) '		\mathbf{i}
	1	Y UI	NO.	Men		201	10) (~)	S A	10	Ľ4	y y	
	1 Sty		A A A A A A A A A A A A A A A A A A A	Wester Clear Dates Life Call		Call said the the		cette adiat		\sim		Aller pick and action
PIC16FR62A ⁽¹⁾	20	¥	128	TMR0,	F	SPI/I ² C		~	8	2.5-6.0	Yes	28-pin SDIP, SOIC, SSOP
				TMR1, TMR2								
PIC16FR63 ⁽¹⁾	20	4	192	TMR0,	2	SPI/I ² C,		10	52	2.5-6.0	Yes	28-pin SDIP, SOIC
				TMR1, TMR2		USART						
PIC16FR64A ⁽¹⁾	20	ž	128	TMR0,	-	SPI/I ² C	Yes	ω	g	2.5-6.0	Yes	40-pin DIP;
			-	TMR1, TMR2								44-pin PLCC, MQFP, TQFP
PIC16FR65	20	4	192	TMR0,	2	SPI/I ² C,	Yes	11	33	2.5-6.0	I	40-pin DIP;
				TMR1, TMR2		USART						44-pin PLCC, MQFP
PIC16FR65A ⁽¹⁾	20	¥	192	TMR0,	N	SPI/I ² C,	Yes	÷	g	2.5-6.0	Yes	40-pin DIP;
				TMR1, TMR2		USART						44-pin PLCC, MQFP, TQFP
All PIC	316/17	family	device	s have Power-o	ñ	eset, selec	ctable \	Natcho	log Til	mer, selec	table c	All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O
curren	current capability	oility.										
Noto 1. Dioner			r loool e	Please sentrot vour legal sales office for availability of these devices	lich	4 to vilide	ap page	avine				

Please contact your local sales office for availability of these devices. ÷ Note

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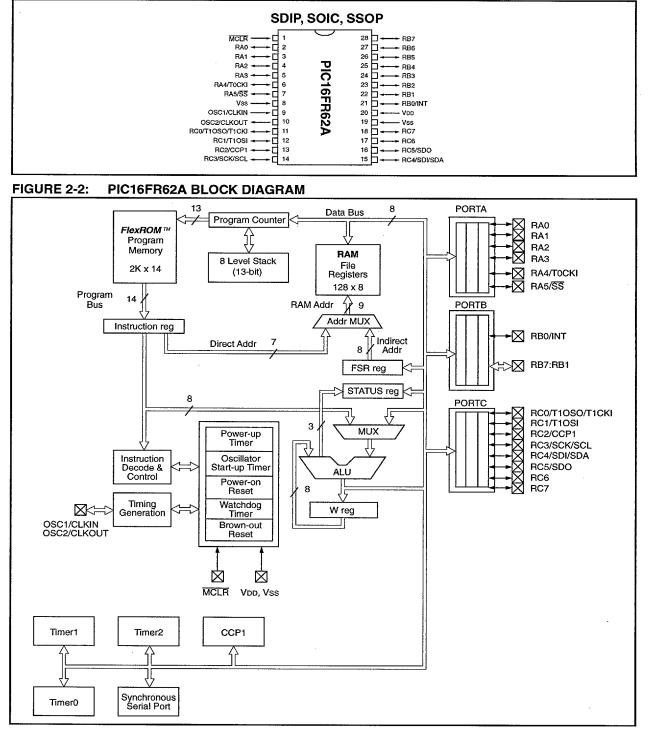
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2.0 PIC16FR62A DEVICE

This section provides information on the architecture of the PIC16FR62A. For information on; operation of the peripherals, electrical specifications etc., please refer to the PIC16C6X data sheet.

FIGURE 2-1: PIC16FR62A PIN DIAGRAM



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TABLE 2-1: PIC16FR62A PINOUT DESCRIPTION

Pin Name	DIP, SSOP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	9	1	ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	0	_	Oscillator crystal output. Connects to crystal or resonator in crys- tal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	1	l/P	ST	Master clear reset input. This pin is an active low reset to the device.
				PORTA is a bi-directional I/O port.
RA0	2	1/O	TTL	
RA1	3	I/O	TTL	
RA2	4	I/O	TTL	
RA3	5	I/O	TTL	
RA4/T0CKI	6	1/0	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	1/O	TTL	Slave select for the synchronous serial port.
· · · · · · · · · · · · · · · · · · ·				PORTB is a bi-directional I/O port. PORTB can be software pro- grammed for internal weak pull-up on all inputs.
RB0/INT	21	1/O	TTL/ST ⁽²⁾	RB0/INT can also be selected as an external interrupt pin.
RB1	22	1/O	TTL	
RB2	23	1/0	TTL	,
RB3	24	1/O	TTL	
RB4	25	1/O	TTL	Interrupt on change pin.
RB5	26	1/0	TTL	Interrupt on change pin.
RB6	27	1/O	TTL	Interrupt on change pin.
RB7	28	I/O	TTL	Interrupt on change pin.
				PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	1/0	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscil- lator output/Timer1 clock input.
RC1/T1OSI	12	I/O	ST	RC1/T1OSI can also be selected as a Timer1 oscillator input
RC2/CCP1	13	1/0	ST	RC2/CCP1 can also be selected as a Capture1 input/ Compare1 output/PWM1 output.
RC3/SCK/SCL	14	1/0	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	15	1/0	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	16	1/0	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6	17	1/0	ST	
RC7	18	1/0	ST	
Vss	8,19	Р		Ground reference for logic and I/O pins.
VDD	20	P		Positive supply for logic and I/O pins.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
 2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

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FIGURE 2-3: PIC16FR62A PROGRAM MEMORY MAP AND STACK

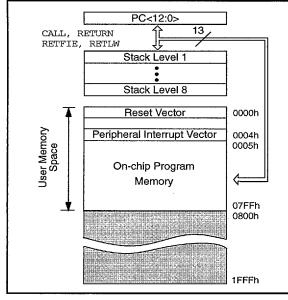
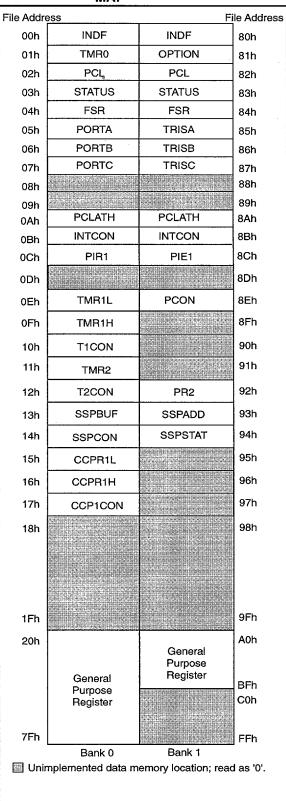


FIGURE 2-4: PIC16FR62A REGISTER FILE MAP



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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 0		-	· · · · · · · · · · · · · · · · · · ·								
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMRO	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data	a memory ac	Idress pointe	e er				L	xxxx xxxx	
05h	PORTA	<u> </u>		PORTA Dat	a Latch wher	n written: PO	RTA pins wh	en read		xx xxxx	uu uuuu
06h	PORTB	PORTB Dat	a Latch whe	n written: PC	ORTB pins w	nen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Dat	ta Latch whe	en written: PC	ORTC pins w	hen read				XXXX XXXX	นนนน นนนน
08h		Unimpleme	nted		raharijina sela Ruhi serterhene						\rightarrow
09h	Ţ	Unimpleme	ener of the second second second second							9 <u>00900-0</u> 54-056	
0Ah ^(1,2)	PCLATH	—		1	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	ан сан сан сан сан сан сан сан сан сан с	1	SSPIF	CCP1IF	TMR2IF	TMR1IF	00 0000	00 0000
ODh	-	Unimpleme	nted								—
0Eh	TMR1L	Holding regi	ister for the I	Least Signific	cant Byte of t	he 16-bit TM	R1 register			xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding regi	ister for the I	Most Signific	ant Byte of th	ne 16-bit TMI	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	- 1		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTP\$2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	is Serial Por	t Receive Bu	iffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	-		CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h-1Fh		Unimplemen	nted								ł

TABLE 2-2: PIC16FR62A SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16FR62A, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved, always maintain these bits clear.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 1	1.	L	8				1		1		I
80h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Sigr	ificant Byte					0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RPO	TO	PD	z	DC -	с	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect dat	a memory ac	ldress pointe	ər		•	•		xxxx xxxx	นบบน บบบน
85h	TRISA			PORTA Dat	a Direction R	egister				11 1111	11 1111
86h	TRISB	PORTB Da	ta Direction I	Register				· .		1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction I	Register						1111 1111	1111 1111
88h		Unimpleme	nted	offender of the							
89h	a succession of the second	Unimpleme	nted					i i bio		-	
8Ah ^(1,2)	PCLATH	—		_	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	(5)	(5)			SSPIE	CCP1IE	TMR2IE	TMR1IE	00 0000	00 0000
8Dh		Unimpleme	nted							_	_
8Eh	PCON		and the second second	an an the state of	ann an thair ann an thair an t	and share the second	1	POR	BOR		uu
8Fh		Unimpleme	nted						and a second second second		-
90h	and a state of the state of the	Unimpleme	nted							<u></u>	<u>—</u>
91h	<u></u>	Unimpleme	nted							<u></u>	
92h	PR2	Timer2 Peri	iod Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	us Serial Por	t (I ² C mode)	Address Reg	ister				0000 0000	0000 0000
94h	SSPSTAT			D/A	Р	S	R/W	UA	BF	00 0000	00 0000
95h-9Fh		Unimpleme	nted								anne <u>n a</u> nns, s

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

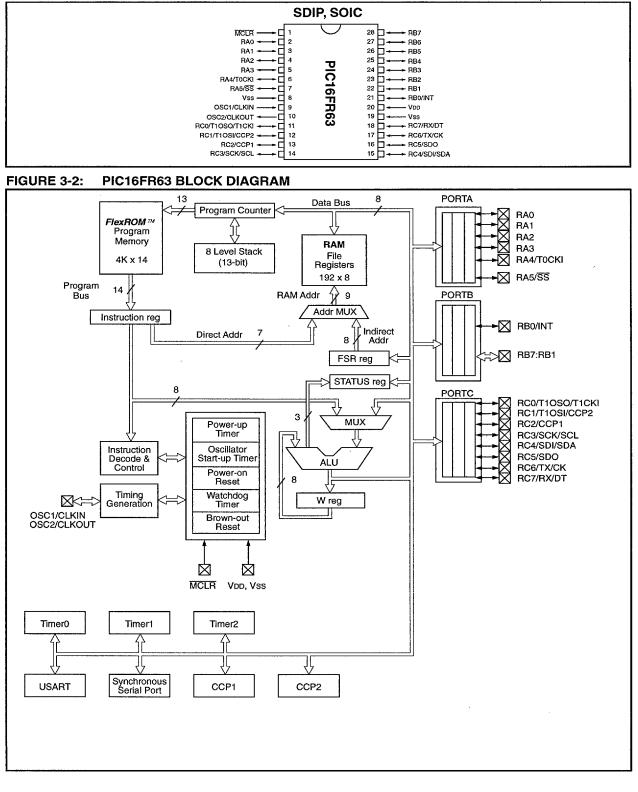
4: The IRP and RP1 bits are reserved on the PIC16FR62A, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved, always maintain these bits clear.

3.0 PIC16FR63 DEVICE

This section provides information on the architecture of the PIC16FR63. For information on; operation of the peripherals, electrical specifications etc., please refer to the PIC16C6X data sheet.

FIGURE 3-1: PIC16FR63 PIN DIAGRAM



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Pin Name	DIP, SSOP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	9	I	ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	0		Oscillator crystal output. Connects to crystal or resonator in crys- tal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	1	I/P	ST	Master clear reset input. This pin is an active low reset to the device.
				PORTA is a bi-directional I/O port.
RA0	2	I/O -	TTL	
RA1	3	1/O	TTL	
RA2	4	I/O	TTL	
RA3	5	1/0	TTL	
RA4/T0CKI	6	1/0	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	1/0	TTL	Slave select for the synchronous serial port.
				PORTB is a bi-directional I/O port. PORTB can be software pro-
				grammed for internal weak pull-up on all inputs.
RB0/INT	21	I/O	TTL/ST ⁽²⁾	RB0/INT can also be selected as an external interrupt pin.
RB1	22	1/O	TTL	
RB2	23	I/O	TTL	
RB3	24	1/O	TTL	
RB4	25	1/0	TTL	Interrupt on change pin.
RB5	26	I/O	TTL	Interrupt on change pin.
RB6	27	1/0	TTL	Interrupt on change pin.
RB7	28	1/0	TTL	Interrupt on change pin.
			••	PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	1/0	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscil- lator output/Timer1 clock input.
RC1/T1OSI/CCP2	12	1/0	ST	RC1/T1OSI can also be selected as a Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	13	1/0	ST	RC2/CCP1 can also be selected as a Capture1 input/ Compare1 output/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	15	1/0	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	16	1/0	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	17	1/0	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or USART Synchronous Clock.
RC7/RX/DT	18	1/0	ST	RC7/RX/DT can also be selected as the Asynchronous Receive or USART Synchronous Data.
Vss	8,19	Р		Ground reference for logic and I/O pins.
VDD	20	Р		Positive supply for logic and I/O pins.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used;TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

FIGURE 3-3: PIC16FR63 PROGRAM MEMORY MAP AND STACK

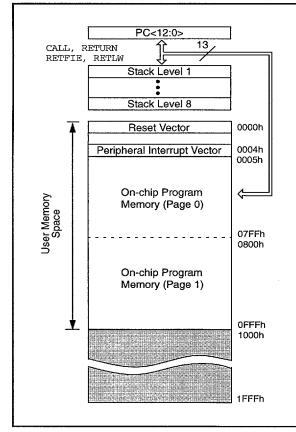


FIGURE 3-4: PIC16FR63 REGISTER FILE MAP

	IVIAP		
File Addre	əss	Fil	e Address
00h	INDF	INDF	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h			88h
09h	PCLATH	PCLATH	89h 8Ah
0Ah 0Ph	INTCON	INTCON	8An 8Bh
0Bh 0Ch	PIR1	PIE1	8Ch
	PIR1 PIR2	PIE1	8Dh
0Dh			
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h	General	General	A0h
7Fh	Purpose Register	Purpose Register	FFh
🔜 Unir	Bank 0 mplemented data m	Bank 1 emory location; read	' i as '0'.

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TABLE 3-2:	PIC16FB63 SPECIAL	FUNCTION REGISTER	SUMMARY
	TIOTOLINO OL LOIAL	TONOTION REGISTER	OOMINIA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 0											
Op/10 INDF Addressing this location uses contents of FSR to address data memory (not a physical register) D1h TMR0 Timer0 module's register D2p(1) PCL Program Counter's (PC) Least Significant Byte D3p(1) STATUS IpP(4) RP1(4) RP0 TO PD Z DC C D3p(1) STATUS IpP(4) RP1(4) RP0 TO PD Z DC C D3p(1) STATUS IpP(4) RP1(4) RP0 TO PD Z DC C D3p(1) STATUS IpP(4) RP1(4) RP0 TO PD Z DC C D3p(1) PORTA PORTA PORTA Data Latch when written: PORTA pins when read Unimplemented Unimplemented Unimplemented Unimplemented Unimplemented Unimplemented E E TOIF INTC RBIE TOIF INTR2 RBIF CP11F TMR1F RBIF CP21F CP21F TMR1F E CP21F CP21F		register)	0000 0000	0000 0000							
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC) Least Signi	ficant Byte				·····.	0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	с	0001 1xxx	000g quuu
04h ⁽¹⁾	FSR	Indirect data	a memory a	dress pointe	er	1	1			xxxx xxxx	บนนน นนนน
05h	PORTA			PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read	·····	xx xxxx	
06h	PORTB	PORTB Dat	a Latch whe	n written: P	ORTB pins w	hen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Dat	a Latch whe	en written: P	ORTC pins w	hen read			· ,	xxxx xxxx	บนนน บนนน
08h	ana in tai an	Unimpleme	nted								_
09h		Unimpleme	nted								
0Ah ^(1,2)	PCLATH	and the second second		<u></u>	Write Buffer	for the uppe				0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	RCIF	TXIF	SSPIF	CCP11F	TMR2IF	TMR1IF	00 0000	00 0000
0Dh	PIR2								CCP2IF	0	0
0Eh	TMR1L	Holding reg	ister for the		1200 12 1200 12 12 12 12 12 12 12 12 12 12 12 12 12					xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding regi								xxxx xxxx	<u>uuuu</u> uuuu
10h	T1CON									00 0000	uu uuuu
11h	TMR2	Timer2 mod								0000 0000	0000 0000
12h	T2CON	ł	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPSO	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	s Serial Por	t Receive Bu	iffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWN	11 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWN	11 (MSB)			-			xxxx xxxx	uuuu uuuu
17h	CCP1CON	-		CCP1X	CCP1Y	1	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	.SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Trai	nsmit Data F	Register						0000 0000	0000 0000
1Ah	RCREG	USART Rec	eive Data F	egister						0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	mpare/PWN	12 (LSB)						XXXXX XXXXX	uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWN	2 (MSB)						xxxx xxxx	นนนน นนนน
1Dh	CCP2CON		11.0 -	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh		Unimpleme	nted							_	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16FR63, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved, always maintain these bits clear.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 1	I	I	L		I	ł				1	
80h ⁽¹⁾	INDF	Addressing	this location	uses conte	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Co	Program Counter's (PC) Least Significant Byte 00								0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	ਰ ਜ	PD	z	DC	с	0001 1xxx	000q quuu
84h(1)	FSR	Indirect date	Indirect data memory address pointer								uuuu uuuu
85h	TRISA	-		PORTA Da	ta Direction F	legister				11 1111	11 1111
86h	TRISB	PORTB Da	ta Direction I	Register						1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction I	Register						1111 1111	1111 1111
88h		Unimpleme	Unimplemented								
89h		191 - S.									
8Ah ^(1,2)	PCLATH	Write Buffer for the upper 5 bits of the Program Counter							0 0000	0 0000	
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	(5)	(5)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2								CCP2IE	0	0
8Eh	PCON		—			—		POR	BOR	qq	uu
8Fh	<u> </u>	Unimpleme	Unimplemented								—
90h		Unimpleme	nted								and the second sec
91h	<u></u>	Unimpleme	nted								
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	us Serial Por	t (I ² C mode)	Address Reo	gister				0000 0000	0000 0000
94h	SSPSTAT			D/Ā	Р	s	R/₩	UA	BF	00 0000	00 0000
95h		Unimpleme	nted								
96h		Unimpleme									1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 - 1999 -
97h	alana an taon ang ang ang ang ang ang ang ang ang an	Unimpleme	nted		1	1	I				
98h ⁽²⁾	TXSTA	CSRC	ТХ9	TXEN	SYNC	-	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h ⁽²⁾	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000
9Ah		Unimpleme									
9Bh	-	Unimpleme			1. Constant					-	
9Ch		Unimpleme	Constant of the second s							1999 <u>- 1</u> 999 -	
9Dh	-	Unimpleme									<u> </u>
9Eh		Unimpleme	respectively and the end of the second s							-	-
9Fh		Unimpleme	nted								-

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16FR63, always maintain these bits clear.

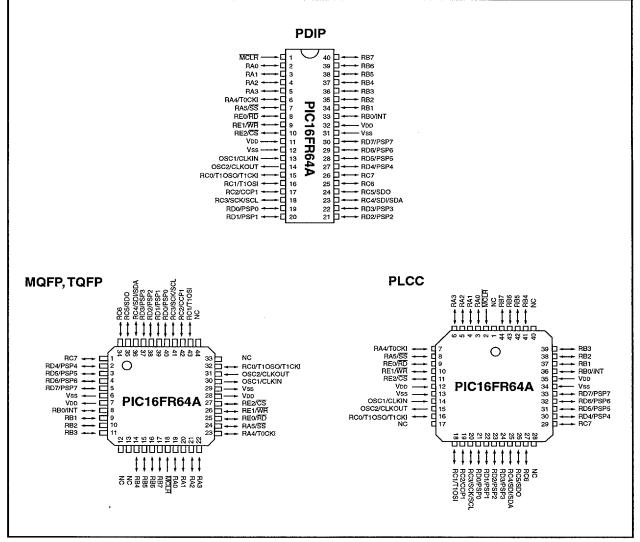
5: PIE1<7:6> and PIR1<7:6> are reserved, always maintain these bits clear.

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4.0 PIC16FR64A DEVICE

This section provides information on the architecture of the PIC16FR64A. For information on; operation of the peripherals, electrical specifications etc., please refer to the PIC16C6X data sheet.





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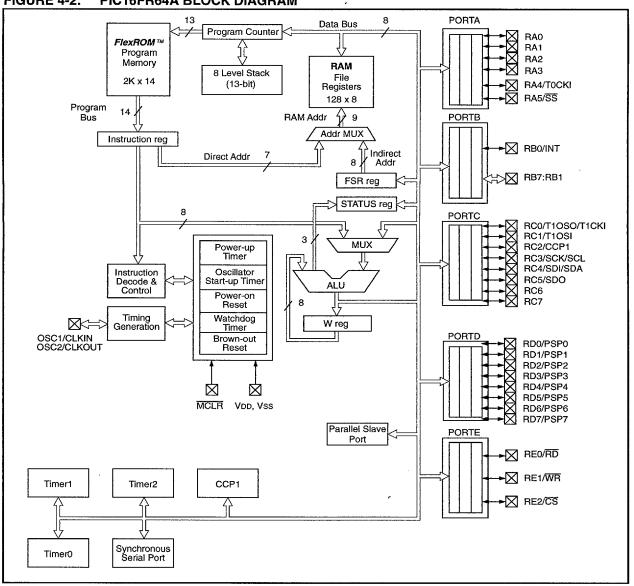
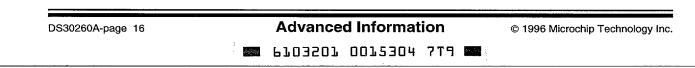


FIGURE 4-2: PIC16FR64A BLOCK DIAGRAM



OSC2/CLKOUT MCLR RA0 RA1 RA2 RA3 RA4/T0CKI RA5/SS	13 14 1 2 3 4 5 6	14 15 2 3 4 5 6	30 31 18 19 20 21	 0 /P /O /O	ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input. Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. Master clear reset input. This pin is an active low reset to the device.
MCLR RA0 RA1 RA2 RA3 RA4/T0CKI RA5/SS	1 2 3 4 5 6	2 3 4 5 6	18 19 20	I/P I/O		in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. Master clear reset input. This pin is an active low reset to the device.
RA0 RA1 RA2 RA3 RA4/T0CKI RA5/SS	2 3 4 5 6	3 4 5 6	19 20	I/O		the device.
RA1 RA2 RA3 RA4/T0CKI RA5/SS	3 4 5 6	4 5 6	20			
RA1 RA2 RA3 RA4/T0CKI RA5/SS	3 4 5 6	4 5 6	20			PORTA is a bi-directional I/O port.
RA2 RA3 RA4/T0CKI RA5/SS	4 5 6	5 6		1/0	TTL	
RA3 RA4/T0CKI RA5/SS	5 6	6	21		TTL	
RA4/T0CKI RA5/SS	6	-		I/O	TTL	
RA5/55	-		22	I/O	TTL	
	I	7	23	I/O	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RB0/INT :	7	8	24	I/O	TTL	Slave select for the synchronous serial port.
RB0/INT						PORTB is a bi-directional I/O port. PORTB can be soft-
RB0/INT					(0)	ware programmed for internal weak pull-up on all inputs.
· · · · · · · · · · · · · · · · · · ·	33	36	8	I/O	TTL/ST ⁽²⁾	RB0/INT can also be selected as an external inter- rupt pin.
RB1 :	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL	Interrupt on change pin.
RB7	40	44	17	1/0	TTL	Interrupt on change pin.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI	16	18	35	I/O	ST	RC1/T1OSI can also be selected as a Timer1 oscil- lator input.
RC2/CCP1	17	19	36	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchro- nous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO 2	24	26	43	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6	25	27	44	I/O	ST	
RC7	26	29	1	I/O	ST	

TABLE 4-1:PIC16FR64A PINOUT DESCRIPTION

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used;TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

Pin Name	DIP Pin#	PLCC Pin#	MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL ⁽³⁾	
RD1/PSP1	20	22	39	I/O	ST/TTL ⁽³⁾	
RD2/PSP2	21	23	40	1/O	ST/TTL ⁽³⁾	
RD3/PSP3	22	24	41	1/0	ST/TTL ⁽³⁾	
RD4/PSP4	27	30	2	1/0	ST/TTL ⁽³⁾	
RD5/PSP5	28	31	3	1/0	ST/TTL ⁽³⁾	
RD6/PSP6	29	32	4	I/O	ST/TTL ⁽³⁾	
RD7/PSP7	30	33	5	I/O	ST/TTL ⁽³⁾	
· · · · · · · · · · · · · · · · · · ·						PORTE is a bi-directional I/O port.
RE0/RD	8	9	25	1/0	ST/TTL ⁽³⁾	RE0/RD read control for parallel slave port.
RE1/WR	9	10	26	I/O	ST/TTL ⁽³⁾	RE1/WR write control for parallel slave port.
RE2/CS	10	11	27	I/O	ST/TTL ⁽³⁾	RE2/CS select control for parallel slave port.
Vss	12,31	13,34	6,29	Р	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	Р	—	Positive supply for logic and I/O pins.
NC	-	1,17, 28,40	12,13, 33,34	_	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; --- = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

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FIGURE 4-3: PIC16FR64A PROGRAM MEMORY MAP AND STACK

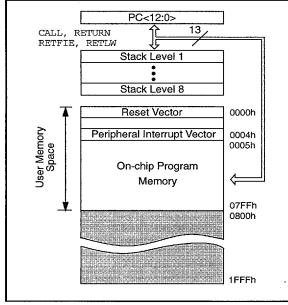


FIGURE 4-4: PIC16FR64A REGISTER FILE MAP

	MAP		
File Addre	ess	Fi	le Address
00h	INDF	INDF	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD	TRISD	88h
09h	PORTE	TRISE	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h			98h
1Fh			9Fh
20h		General	A0h
		Purpose	
	General Purpose	Register	BFh
	Register		C0h
7Fh			FFh
	Bank 0	Bank 1	
💹 Unir	nplemented data m	emory location; read	l as '0'.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 0											
00h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000
01h	TMR0	Timer0 module's register									uuuu uuuu
02h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	то	PD	z	DC	С	0001 1xxx	000g guuu
_{04h} (1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA		PORTA Data Latch when written: PORTA pins when read								uu uuuu
06h	PORTB	PORTB Dat	PORTB Data Latch when written: PORTB pins when read								uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read									uuuu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read									uuuu uuuu
09h	PORTE	_				—	RE2	RE1	RE0	xxx	uuu
0Ah ^(1,2)	PCLATH	Write Buffer for the upper 5 bits of the Program Counter								0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(5)		<u> </u>	SSPIF	CCP1IF	TMR2IF	TMR1IF	00 0000	00 0000
0Dh	1	Unimpleme	nted								
0Eh	TMR1L	Holding reg	ister for the l	east Signific	cant Byte of t	he 16-bit TM	R1 register			xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the I	Most Signific	ant Byte of th	ne 16-bit TMI	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON		l	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	-	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	is Serial Port	Receive Bu	iffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	-	an a	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h-1Fh		Unimpleme	nted								

TABLE 4-2: PIC16FR64A SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16FR64A, always maintain these bits clear.

5: PIE1<6> and PIR1<6> are reserved on the PIC16FR64A, always maintain these bits clear.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾
Bank 1	L	1	unic -								
80h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physica	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	RPO TO PD Z DC C 0			0001 1xxx	000q quuu		
84h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA		PORTA Data Direction Register								
86h	TRISB	PORTB Data Direction Register									1111 1111
87h	TRISC	PORTC Data Direction Register									1111 1111
88h	TRISD	PORTD Data Direction Register									1111 1111
89h	TRISE	IBF	IBF OBF IBOV PSPMODE TRISE2 TRISE1 TRISE0								0000 -111
8Ah ^(1,2)	PCLATH			ł	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(5)	1		SSPIE	CCP1IE	TMR2IE	TMR1IE	00 0000	00 0000
8Dh		Unimpleme	nted								
8Eh	PCON		-	[. <u> </u>	—	1	POR	BOR	qq	uu
8Fh		Unimpleme	nted							—	
90h		Unimpleme	nted								<u> </u>
91h	<u></u>	Unimpleme	nted							-	
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	is Serial Por	t (I ² C mode)	Address Reg	jister				0000 0000	0000 0000
94h	SSPSTAT		19. se <u></u> 1988	D/Ā	Р	S	R/₩	UA	BF	00 0000	00 0000
95h-9Fh		Unimpleme	nted							_	-

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

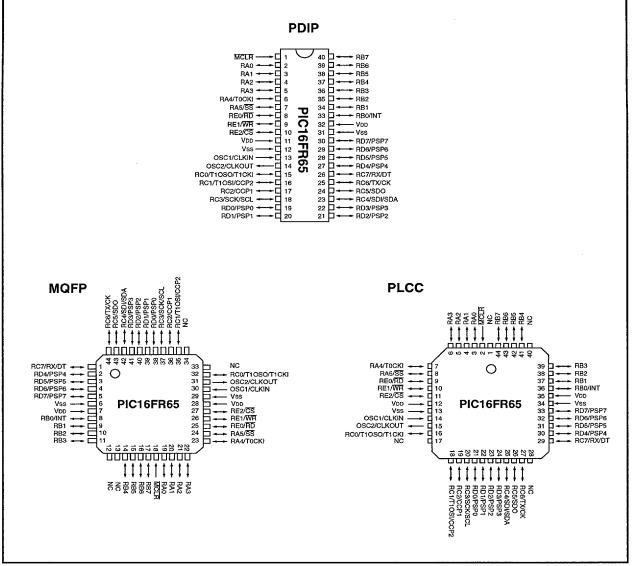
4: The IRP and RP1 bits are reserved on the PIC16FR64A, always maintain these bits clear.

5: PIE1<6> and PIR1<6> are reserved on the PIC16FR64A, always maintain these bits clear.

5.0 PIC16FR65 DEVICE

This section provides information on the architecture of the PIC16FR65. For information on; operation of the peripherals, electrical specifications etc., please refer to the PIC16C6X data sheet.





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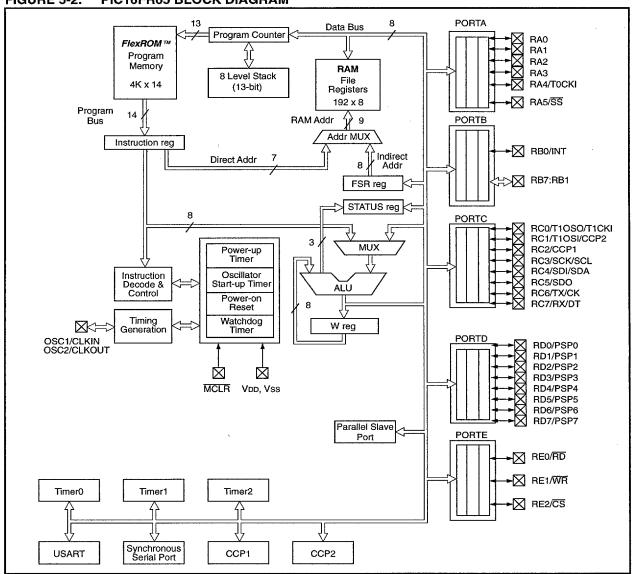


FIGURE 5-2: PIC16FR65 BLOCK DIAGRAM

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Pin Name	DIP Pin#	PLCC Pin#	MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	1	ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	1	2	18	I/P	ST	Master clear reset input. This pin is an active low reset to the device.
		-				PORTA is a bi-directional I/O port.
RAO	2	3	19	1/0	TTL	
RA1	3	4	20	1/0	TTL	
RA2	4	5	21	1/0	TTL	
RA3	5	6	22	1/0	TTL	
RA4/T0CKI	6	7	23	1/0	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	8	24	1/0	TTL	Slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be soft- ware programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	1/0	TTL/ST ⁽²⁾	RB0/INT can also be selected as an external inter- rupt pin.
RB1	34	37	9	1/0	TTL	
RB2	35	38	10	1/0	TTL	
RB3	36	39	11	1/0	TTL	
RB4	37	41	14	1/0	TTL	Interrupt on change pin.
RB5	38	42	15	1/0	TTL	Interrupt on change pin.
RB6	39	43	16	1/0	TTL	Interrupt on change pin.
RB7	40	44	17	1/0	TTL	Interrupt on change pin.
					1	PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	1/0	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1/T1OSI/CCP2 can also be selected as a Timer1 oscillator input or Capture2 input/Compare2 output/ PWM2 output.
RC2/CCP1	17	19	36	1/0	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchro- nous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	23	25	42	1/0	ST	RC4/SDI/SDA can also be selected as the SPI Data in (SPI mode) or data I/O (I ² C mode).
RC5/SDO	24	26	43	1/0	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	1/0	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or USART Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7/RX/DT can also be selected as the Asynchro- nous Receive or USART Synchronous Data.

TABLE 5-1: PIC16FR65 PINOUT DESCRIPTION

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

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Pin Name	DIP Pin#	PLCC Pin#	MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL ⁽³⁾	
RD1/PSP1	20	22	39	I/O	ST/TTL ⁽³⁾	
RD2/PSP2	21	23	40	I/O	ST/TTL ⁽³⁾	
RD3/PSP3	22	24	41	I/O	ST/TTL ⁽³⁾	
RD4/PSP4	27	30	2	1/0	ST/TTL ⁽³⁾	
RD5/PSP5	28	31	3	i/O	ST/TTL ⁽³⁾	
RD6/PSP6	29	32	4	I/O	ST/TTL ⁽³⁾	
RD7/PSP7	30	33	5	I/O	ST/TTL ⁽³⁾	
						PORTE is a bi-directional I/O port.
RE0/RD	8	9	25	I/O	ST/TTL ⁽³⁾	RE0/RD read control for parallel slave port.
RE1/WR	9	10	26	I/O	ST/TTL ⁽³⁾	RE1/WR write control for parallel slave port.
RE2/CS	10	11	27	I/O	ST/TTL ⁽³⁾	RE2/CS select control for parallel slave port.
Vss	12,31	13,34	6,29	Р		Ground reference for logic and I/O pins.
Vdd	11,32	12,35	7,28	P .		Positive supply for logic and I/O pins.
NC	-	1,17, 28,40	12,13, 33,34	_		These pins are not internally connected. These pins should be left unconnected.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used;TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

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FIGURE 5-3: PIC16FR65 PROGRAM MEMORY MAP AND STACK

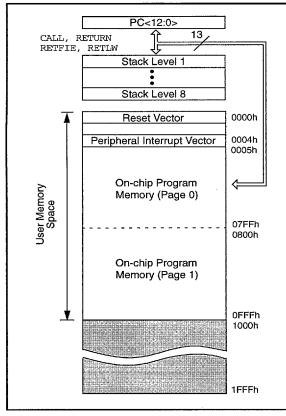


FIGURE 5-4: PIC16FR65 REGISTER FILE

	MAP		
File Addre	ess	Fil	e Address
00h	INDF	INDF	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD	TRISD	88h
09h	PORTE		89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h	General	General	A0h
756	Purpose Register	Purpose Register	FFL
7Fh	Bank 0	Bank 1] FFh
🔳 Unir		emory location; read	d as '0'.

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TABLE 5-2:	PIC16FR65 SPECIAL	FUNCTION REGISTER	SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾			
Bank 0	••••••••••••••••••••••••••••••••••••••			·,										
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000			
01h	TMR0	Timer0 mod	mer0 module's register xxxx xxxx											
02h ⁽¹⁾	PCL	Program Co	ogram Counter's (PC) Least Significant Byte 0000 0000											
03h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	IRP ⁽⁵⁾ RP1 ⁽⁵⁾ RP0 TO PD Z DC C											
_{04h} (1)	FSR	Indirect data	Indirect data memory address pointer											
05h	PORTA	-		PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read		xx xxxx	uu uuuu			
06h	PORTB	PORTB Dat	a Latch whe	en written: PC	ORTB pins w	hen read				xxxx xxxx	uuuu uuuu			
07h	PORTC	PORTC Dat	ta Latch whe	en written: PC	DRTC pins w	hen read				xxxx xxxx	uuuu uuuu			
08h	PORTD	PORTD Dat	ta Latch whe	en written: PC	ORTD pins w	hen read				xxxx xxxx	uuuu uuuu			
09h	PORTE			-	—	1	RE2	RE1	RE0	xxx	uuu			
0Ah ^(1,2)	PCLATH				Write Buffer	for the upper	r 5 bits of th	e Program C	ounter	0 0000	0 0000			
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u			
0Ch	PIR1	PSPIF	(6)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000			
0Dh	PIR2							-	CCP2IF	0	0			
0Eh	TMR1L	Holding reg	ister for the	Least Signific	cant Byte of t	he 16-bit TM	R1 register	1.0000000000000000000000000000000000000		xxxx xxxx	uuuu uuuu			
0Fh	TMR1H	Holding reg	ister for the	Most Signific	ant Byte of t	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu			
10h	T1CON		1	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu			
11h	TMR2	Timer2 mod	lule's registe)r						0000 0000	0000 0000			
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000			
13h	SSPBUF	Synchronou	is Serial Por	t Receive Bu	Iffer/Transmi	Register				xxxx xxxx	uuuu uuuu			
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000			
15h	CCPR1L	Capture/Co	mpare/PWN	11 (LSB)						XXXX XXXX	uuuu uuuu			
16h	CCPR1H	a material a delas as ana ta	mpare/PWN	11 (MSB)						XXXX XXXX	uuuu uuuu			
17h	CCP1CON		-	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000			
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x			
19h	TXREG	USART Tra	nsmit Data F	Register						0000 0000	0000 0000			
1Ah	RCREG	USART Red	ceive Data F	legister				<u></u>		0000 0000	0000 0000			
1Bh	CCPR2L	Capture/Co	mpare/PWN	12 (LSB)						xxxx xxxx	uuuu uuuu			
1Ch	CCPR2H	Capture/Co	mpare/PWN	12 (MSB)						xxxx xxxx	uuuu uuuu			
1Dh	CCP2CON	-		CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000			
1Eh-1Fh	1	Unimpleme	nted							· —				

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The PCON<0> bit is reserved on the PIC16FR65, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16FR65, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16FR65, always maintain these bits clear.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾		
Bank 1													
80h ⁽¹⁾	INDF	Addressing	Addressing this location uses contents of FSR to address data memory (not a physical register)										
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111		
82h ⁽¹⁾	PCL	Program Co	Program Counter's (PC) Least Significant Byte										
83h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	IRP ⁽⁵⁾ RP1 ⁽⁵⁾ RP0 TO PD Z DC C										
84h ⁽¹⁾	FSR	Indirect dat	a memory ac	ldress point	er	•		•		xxxx xxxx	uuuu uuuu		
85h	TRISA			PORTA Da	ta Direction R	legister				11 1111	11 1111		
86h	TRISB	PORTB Da	ta Direction I	Register	-					1111 1111	1111 1111		
87h	TRISC	PORTC Da	ta Direction I	Register						1111 1111	1111 1111		
88h	TRISD	PORTD Da	ta Direction I	Register						1111 1111	1111 1111		
89h	TRISE	IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0	0000 -111	0000 -111		
8Ah ^(1,2)	PCLATH				Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000		
8Bh(1)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u		
8Ch	PIE1	PSPIE	(6)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000		
8Dh	PIE2							nacia de profesion Succes to d esentos	CCP2IE	0	0		
8Eh	PCON		<u> </u>					POR	(4)	dd	uu		
8Fh		Unimpleme	nted										
90h	—	Unimpleme	nted							—	1		
91h		Unimpleme	nted								-		
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111		
93h	SSPADD	Synchronou	us Serial Por	t (I ² C mode	Address Reg	gister				0000 0000	0000 0000		
94h	SSPSTAT			D/A	Р	s	R/W	UA	BF	00 0000	00 0000		
95h	_	Unimpleme	nted								—		
96h		Unimpleme	nted										
97h		Unimpleme	nted	r	r		1	r	r	-			
98h	TXSTA	CSRC	ТХ9	TXEN	SYNC		BRGH	TRMT	TX9D	0000 -010	0000 -010		
99h	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000		
9Ah	-	Unimpleme	nted								_		
9Bh		Unimpleme	nted										
9Ch		Unimpleme	nted										
9Dh		Unimpleme	nted								1999 - 1999 -		
9Eh		Unimpleme	nted										
9Fh		Unimpleme	nted					a neutroneur nag		ansie — ander			

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The PCON<0> bit is reserved on the PIC16FR65, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16FR65, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16FR65, always maintain these bits clear.

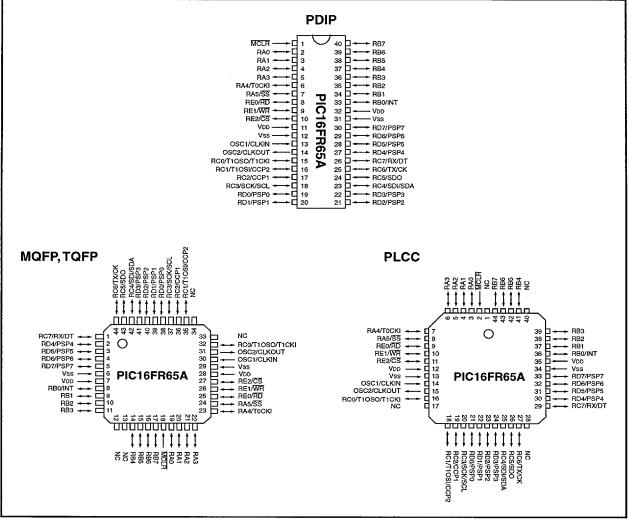
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6.0 PIC16FR65A DEVICE

This section provides information on the architecture of the PIC16FR65A. For information on; operation of the peripherals, electrical specifications etc., please refer to the PIC16C6X data sheet.

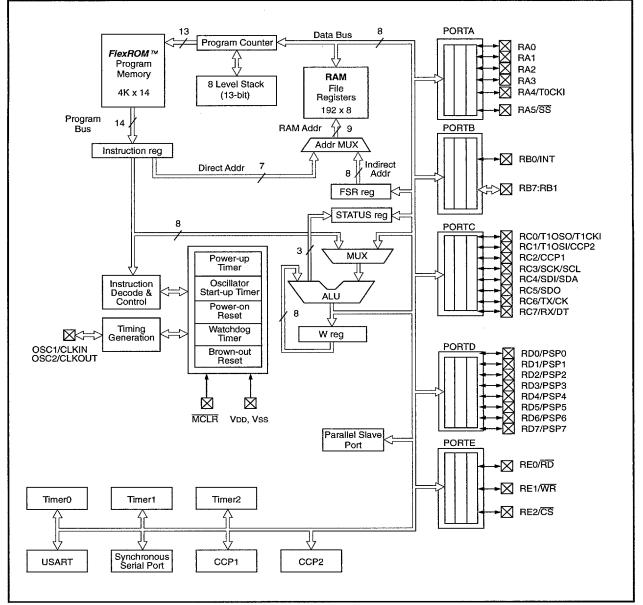




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Pin Name	DIP Pin#	PLCC Pin#	MQFP TQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	ł	ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	1	2	18	I/P	ST	Master clear reset input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	2	3	19	1/0	TTL	
RA1	3	4	20	1/0	TTL	
RA2	4	5	21	1/0	TTL	
RA3	5	6	22	1/0	TTL	
RA4/T0CKI	6	7	23	1/0	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	8	24	1/0	TTL	Slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be soft- ware programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST ⁽²⁾	RB0/INT can also be selected as an external inter- rupt pin.
RB1	34	37	9	1/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	1/0	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	1/0	TTL	Interrupt on change pin.
RB7	40	44	17	1/0	TTL	Interrupt on change pin.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	1/0	ST	RC1/T1OSI/CCP2 can also be selected as a Timer1 oscillator input or Capture2 input/Compare2 output/ PWM2 output.
RC2/CCP1	17	19	36	1/0	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	1/0	ST	RC3/SCK/SCL can also be selected as the synchro- nous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	23	25	42	1/0	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	24	26	43	1/0	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	1/0	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or USART Synchronous Clock.
RC7/RX/DT	26	29	1	1/0	ST	RC7/RX/DT can also be selected as the Asynchro- nous Receive or USART Synchronous Data.

TABLE 6-1: PIC16FR65A PINOUT DESCRIPTION	TABLE 6-1:	PIC16FR65A	PINOUT	DESCRIPTION
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Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used;TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

Pin Name	DIP Pin#	PLCC Pin#	MQFP TQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL ⁽³⁾	
RD1/PSP1	20	22	39	I/O	ST/TTL ⁽³⁾	
RD2/PSP2	21	23	40	I/O	ST/TTL ⁽³⁾	
RD3/PSP3	22	24	41	I/O	ST/TTL ⁽³⁾	
RD4/PSP4	27	30	2	I/O	ST/TTL ⁽³⁾	
RD5/PSP5	28	31	3	I/O	ST/TTL ⁽³⁾	
RD6/PSP6	29	32	4	I/O	ST/TTL ⁽³⁾	
RD7/PSP7	30	33	5	I/O	ST/TTL ⁽³⁾	
						PORTE is a bi-directional I/O port.
RE0/RD	8	9	25	I/O	ST/TTL ⁽³⁾	RE0/RD read control for parallel slave port.
RE1/WR	9	10	26	I/O	ST/TTL ⁽³⁾	RE1/WR write control for parallel slave port.
RE2/CS	10	.11	27	I/O	ST/TTL ⁽³⁾	RE2/CS select control for parallel slave port.
Vss	12,31	13,34	6,29	Р		Ground reference for logic and I/O pins.
Vdd	11,32	12,35	7,28	Р		Positive supply for logic and I/O pins.
NC	-	1,17, 28,40	12,13, 33,34	-		These pins are not internally connected. These pins should be left unconnected.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used;TTL = TTL input; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

FIGURE 6-3: PIC16FR65A PROGRAM MEMORY MAP AND STACK

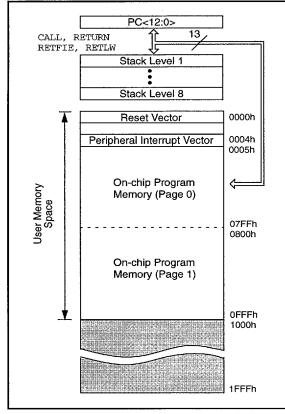


FIGURE 6-4: PIC16FR65/

PIC16FR65A REGISTER FILE

	MAP		
File Addre	ess	Fil	e Address
00h	INDF	INDF	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD	TRISD	88h
09h	PORTE	TRISE	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H	All the second sec	9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h	General	General	A0h
7Fh	Purpose Register	Purpose Register	FFh
	Bank 0	Bank 1	1
🗐 Unir	nplemented data m	emory location; read	1 as '0'.

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TABLE 6-2: PIC16FR65A SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾			
Bank 0										······				
00h ⁽¹⁾	INDF	Addressing	this location	l register)	0000 0000	0000 0000								
01h	TMR0	Timer0 mod	ner0 module's register xxxx xxxx uuuu											
02h ⁽¹⁾	PCL	Program Co	ogram Counter's (PC) Least Significant Byte 0000 0000 0000 0000 0000 0000 0000 0											
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	то	PD	Z	DC	с	0001 1xxx	000q quuu			
_{04h} (1)	FSR	Indirect data	a memory ac	dress pointe	ər	L			L.,	xxxxx xxxxx	uuuu uuuu			
05h	PORTA			PORTA Dat	a Latch wher	n written: PO	RTA pins wh	en read		xx xxxx	uu uuuu			
06h	PORTB		ta Latch whe	n written: PC	ORTB pins wi	nen read				xxxx xxxx	uuuu uuuu			
07h	PORTC	PORTC Dat	ta Latch whe	en written: P	ORTC pins w	hen read				xxxx xxxx	uuuu uuuu			
08h	PORTD	PORTD Dat	ta Latch whe	en written: P	ORTD pins w	hen read				xxxx xxxx	uuuu uuuu			
09h	PORTE	_					RE2	RE1	RE0	xxx	uuu			
0Ah ^(1,2)	PCLATH		<u></u>		Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0:0000	0 0000			
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u			
0Ch	PIR1	PSPIF	(5)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000			
0Dh	PIR2		-			-	ł	-	CCP2IF	0	0			
0Eh	TMR1L	Holding reg	ister for the	Least Signifi	cant Byte of t	he 16-bit TM	R1 register	Line and the second		xxxx xxxx	uuuu uuuu			
0Fh	TMR1H	Holding reg	ister for the	Most Signific	ant Byte of th	ne 16-bit TMI	R1 register			xxxx xxxx	uuuu uuuu			
10h	T1CON	11 A	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu			
11h	TMR2	Timer2 mod	iule's registe	۶r						0000 0000	0000 0000			
12h	T2CON	1	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000			
13h	SSPBUF	Synchronou	us Serial Por	t Receive Bu	uffer/Transmit	Register				xxxx xxxx	11111 11111			
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPMO	0000 0000	0000 0000			
15h	CCPR1L	Capture/Co	mpare/PWN	11 (LSB)						****	uuuu uuuu			
16h	CCPR1H	Capture/Co	mpare/PWN	11 (MSB)					•	xxxx xxxx	uuuu uuuu			
17h	CCP1CON		2011 2018 and 10000	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000			
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x			
19h	TXREG	USART Tra	nsmit Data F	Register						0000 0000	0000 0000			
1Ah	RCREG	USART Red	ceive Data R	legister			ä			0000 0000	0000 0000			
1Bh	CCPR2L	Capture/Co	mpare/PWN	12 (LSB)						xxxx xxxx	uuuu uuuu			
1Ch	CCPR2H	Capture/Co	mpare/PWN	12 (MSB)				<u></u>		xxxx xxxx	uuuu uuuu			
1Dh	CCP2CON			CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000			
1Eh-1Fh		Unimpleme	nted											

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16FR65A, always maintain these bits clear.

5: PIE1<6> and PIR1<6> are reserved on the PIC16FR65A, always maintain these bits clear.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR BOR	Value on all other resets ⁽³⁾		
Bank 1	1			· · · ·									
80h ⁽¹⁾	INDF	Addressing	Addressing this location uses contents of FSR to address data memory (not a physical register)										
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111		
82h ⁽¹⁾	PCL	Program Co	0000 0000	0000 0000									
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	0001 1xxx	000q quuu									
_{84h} (1)	FSR	Indirect dat	a memory ac	dress point	er		•	•		xxxx xxxx	uuuu uuuu		
85h	TRISA			PORTA Da	ta Direction R	legister				11 1111	11 1111		
86h	TRISB	PORTB Da	ta Direction I	Register						1111 1111	1111 1111		
87h	TRISC	PORTC Da	ta Direction	Register						1111 1111	1111 1111		
88h	TRISD	PORTD Da	ta Direction	Register						1111 1111	1111 1111		
89h	TRISE	IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISEO	0000 -111	0000 -111		
8Ah ^(1,2)	PCLATH				Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000		
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u		
8Ch	PIE1	PSPIE	(5)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000		
8Dh	PIE2							-	CCP2IE	0	0		
8Eh	PCON				-			POR	BOR	dd	uu		
8Fh		Unimpleme	nted										
90h	andron ganerad 	Unimpleme	nted	allogic de chie Administration		na kata na santa Kata da kata na ta		rekori peri danan Distrikti ingener	inungi naveni ana	on a transmit	ang na kana panang Kang na kana panang		
91h	100 J.—20 S.	Unimpleme	nted								-		
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111		
93h	SSPADD	Synchronou	us Serial Por	t (I ² C mode)	Address Reg	gister	-			0000 0000	0000 0000		
94h	SSPSTAT	<u></u>	anta n tana	D/Ã	Р	s	R/₩	UA	BF	00 0000	00 0000		
95h	_	Unimpleme	nted							<u> </u>			
96h		Unimpleme	nted										
97h		Unimpleme	nted	F	T		1	1		<u>—</u>	—		
98h	TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D	0000 -010	0000 -010		
99h	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000		
9Ah		Unimpleme	nted										
9Bh		Unimpleme								· · · · · · · · · · · · · · · · · · ·	norma <u>–</u> territori		
9Ch		Unimpleme	nted							<u> </u>	-		
9Dh	-	Unimpleme									-		
9Eh		Unimpleme			anora anatina i						-		
9Fh	. — — — — — — — — — — — — — — — — — — —	Unimpleme	nted							-	—		

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

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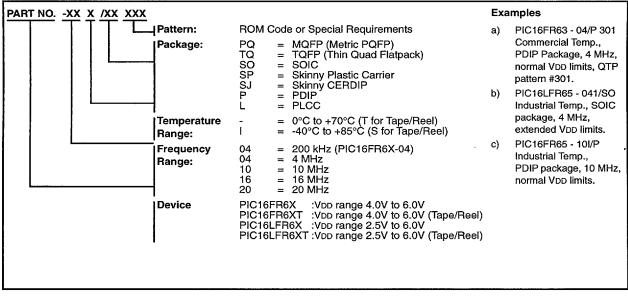
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